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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-27. (cancelled)

28. (new) A clock comprising:

a slave clock including a microprocessor and adapted to be coupled to a master clock;

the microprocessor coupled to a memory, a manually-operable control device, a time display and a diagnostic indicator display;

the microprocessor further configured to receive commands from the master clock;

data and diagnostic software instructions stored in the memory,

whereas, upon operation of the control device at the slave clock, or upon receipt of a command from the master clock, the instructions cause the microprocessor to enter a diagnostics mode, to execute semi-automatic diagnostic self-tests on current status and operability or inoperability of components and functions of the slave clock, to display results of the self-tests via the diagnostic indicator display, and to return the slave clock to a normal clock mode following completion of the self-tests;

the diagnostic self-tests including at least three of the following: determination of communication protocol type used by the slave clock, determination of an ability or inability of the slave clock to receive data from the master clock, determination of motor and drive gear operability or inoperability, determination of current software version in use by the slave clock, determination of presence or absence of electrical power from a power supply, determination

of whether a signal is being received from an optical switch at the slave clock, determination of whether data can be properly read into and out of the memory at the slave clock, and determination of how much time has passed since the slave clock received a communication from the master clock.

29. (new) A master/ slave clock system comprising:

a master clock;

at least one slave clock including a microprocessor and coupled to the master clock;

the microprocessor coupled to a memory, a manually-operable control device, a time display and a diagnostic indicator display; and

data and diagnostic software instructions stored in the memory;

whereas, upon operation of the control device at the slave clock or upon receipt by the slave clock of a command from the master clock, the instructions in the memory cause the microprocessor to enter a diagnostics mode, to execute semi-automatic diagnostic self-tests on current status and operability or inoperability of components and functions of the slave clock, to display results of the tests via the diagnostic indicator display, and to return the slave clock to a normal clock mode following completion of said self-tests;

said diagnostic self-tests including at least three of the following: determination of communication protocol type used by the slave clock, determination of an ability or inability of the slave clock to receive data from the master clock, determination of motor and drive gear operability or inoperability, determination of current software version in use by the slave clock, determination of presence or absence of electrical power from a power supply, determination

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of whether a signal is being received from an optical switch at the slave clock, determination of whether data can be properly read into and out of the memory at the slave clock, and determination of how much time has passed since the slave clock received a communication from the master clock.

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